GENERAL FRONT END ARCHITECTURE

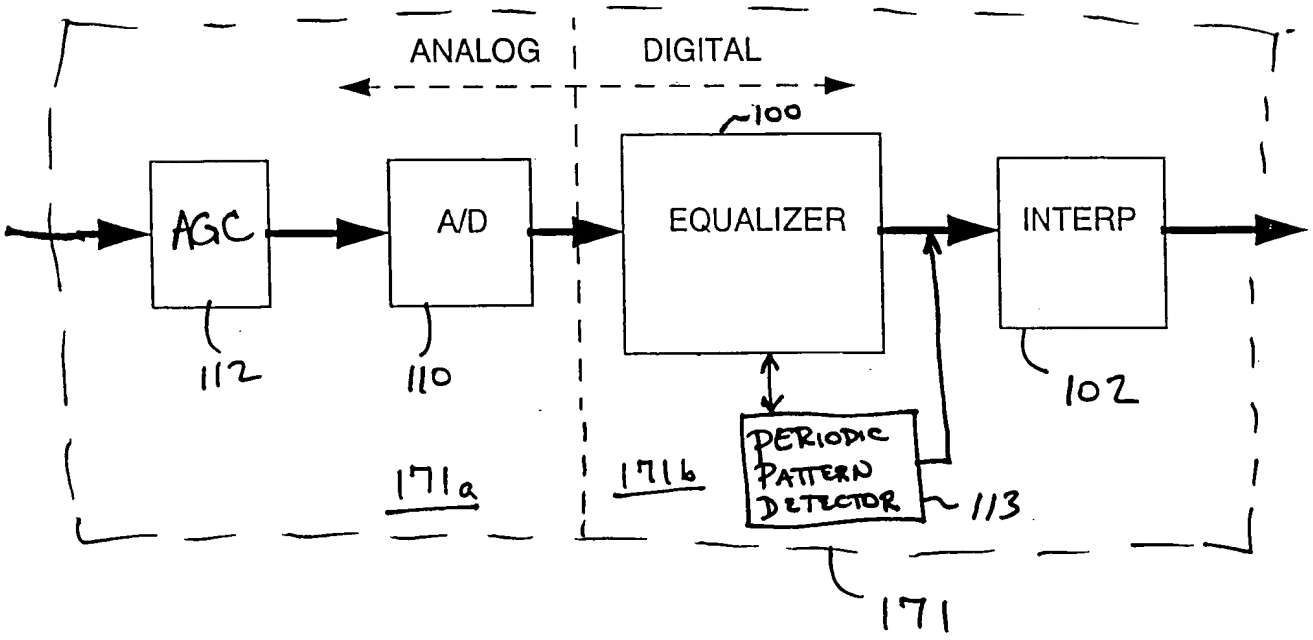


FIG. 1

EQUALIZER ARCHITECTURE

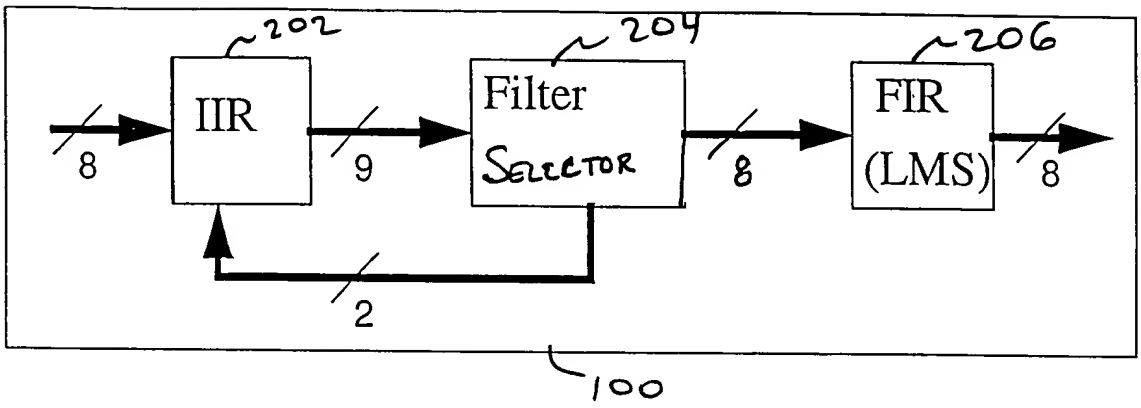


FIG. 2

IIR Filter Block Description

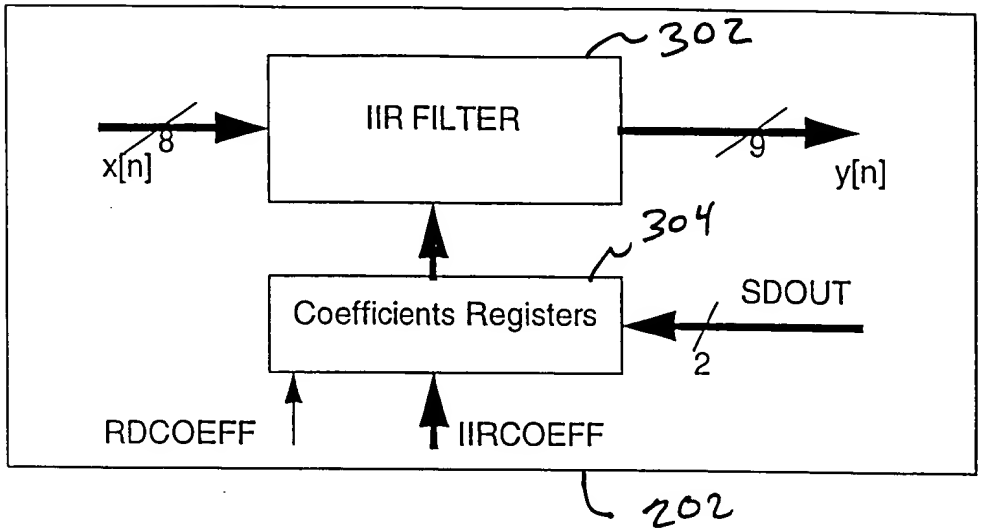


FIG. 3

IIR Filter Block Implementation

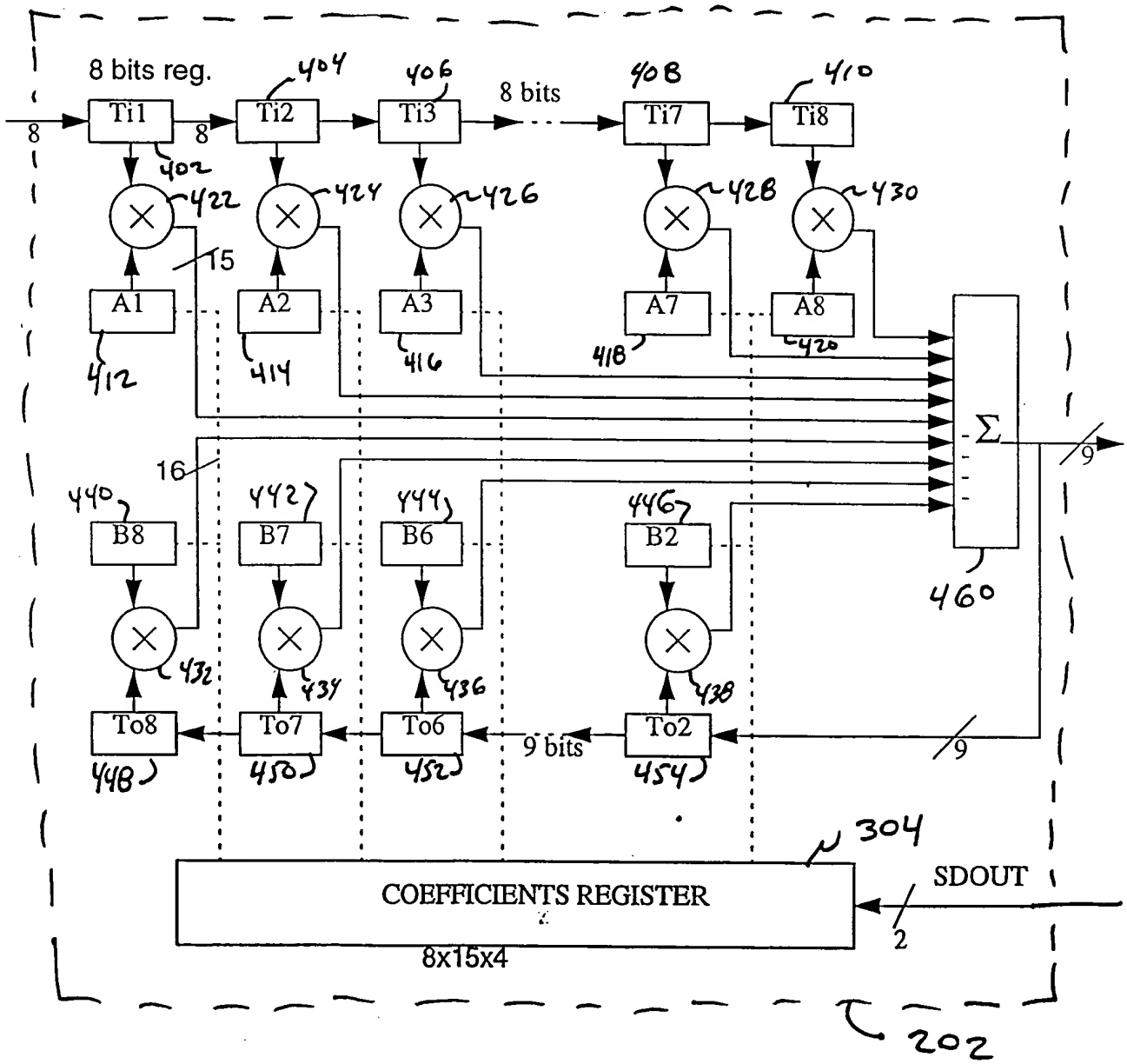


FIG. 4

Filter Selection Block Description

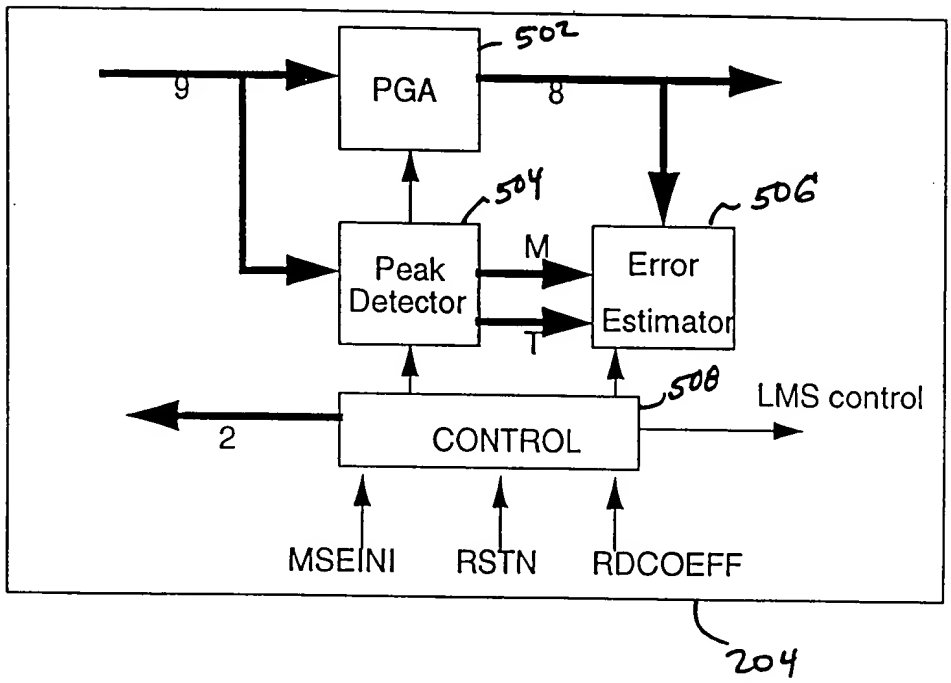
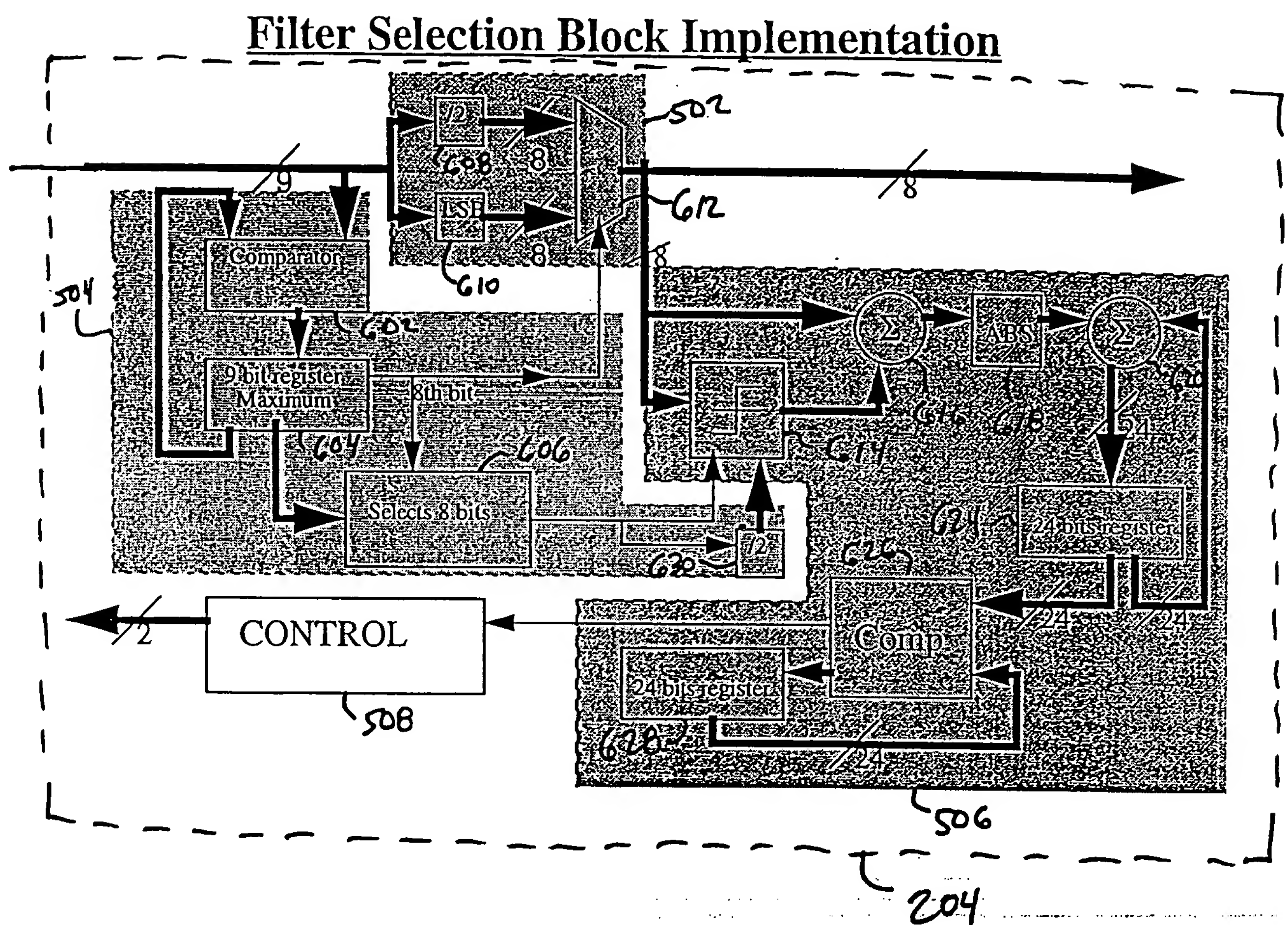


FIG. 5


Filter Selection Block Implementation
/2
LSB
Comparator
9 bit register
Maximum
8th bit
Selects 8 bits
ABS
24 bits register
Comp
24 bits register
CONTROL
9
8
2
24
502
504
506
508
602
604
606
608
610
612
614
616
618
620
624
626
628
630
204

F1G. 6

Adaptive FIR Filter Description

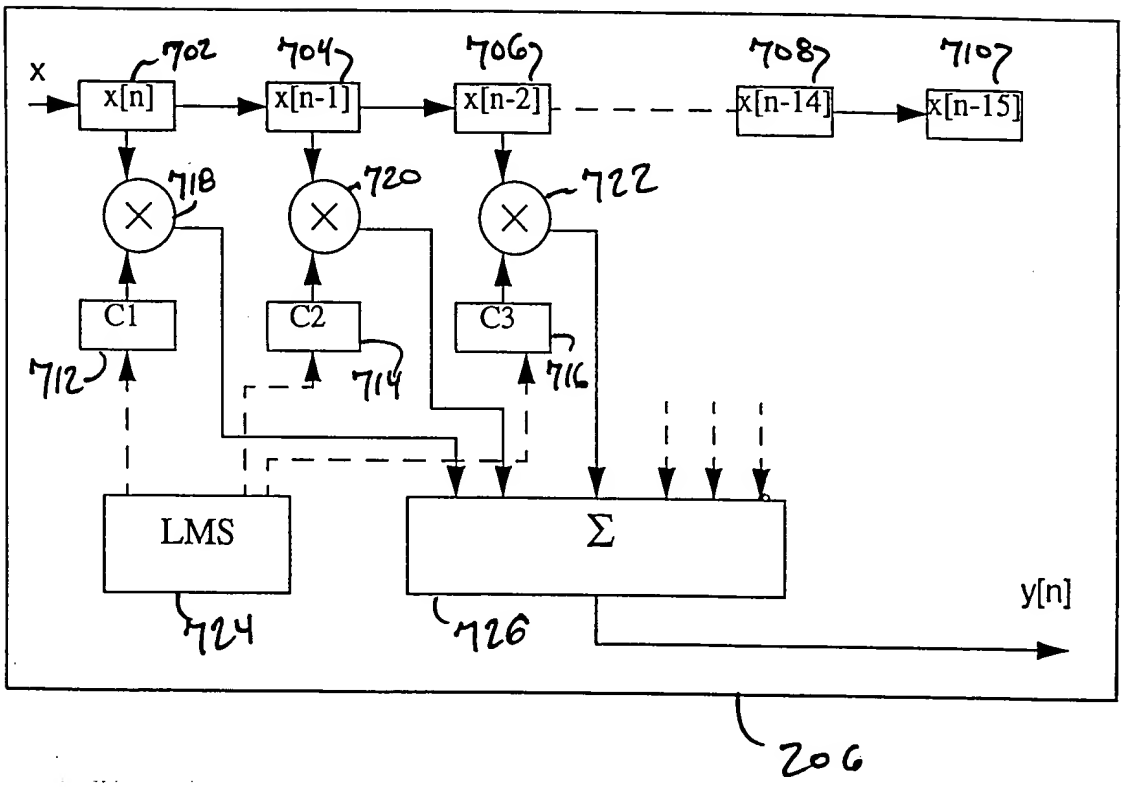


FIG. 7

Adaptive FIR Filter Block Implementation

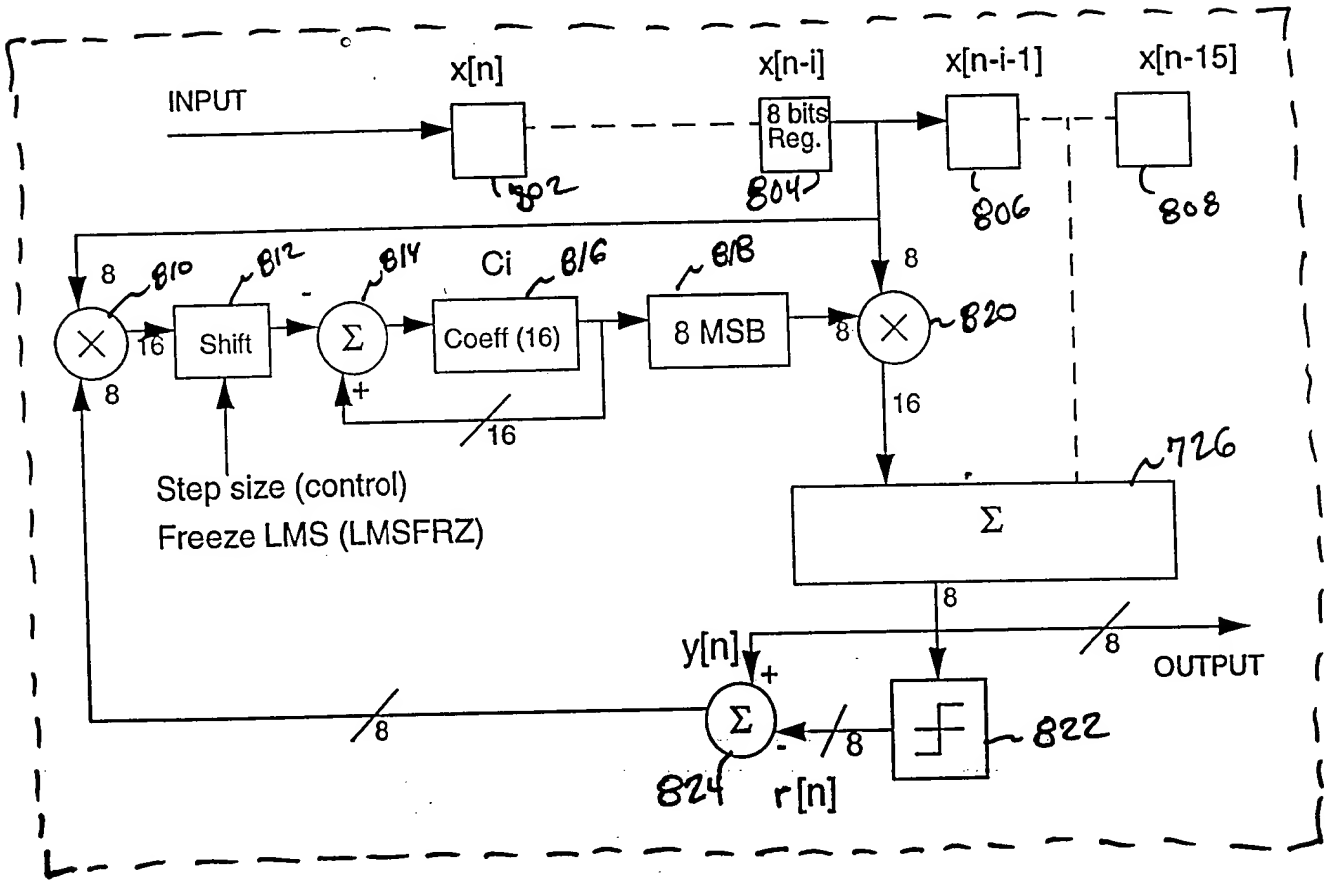
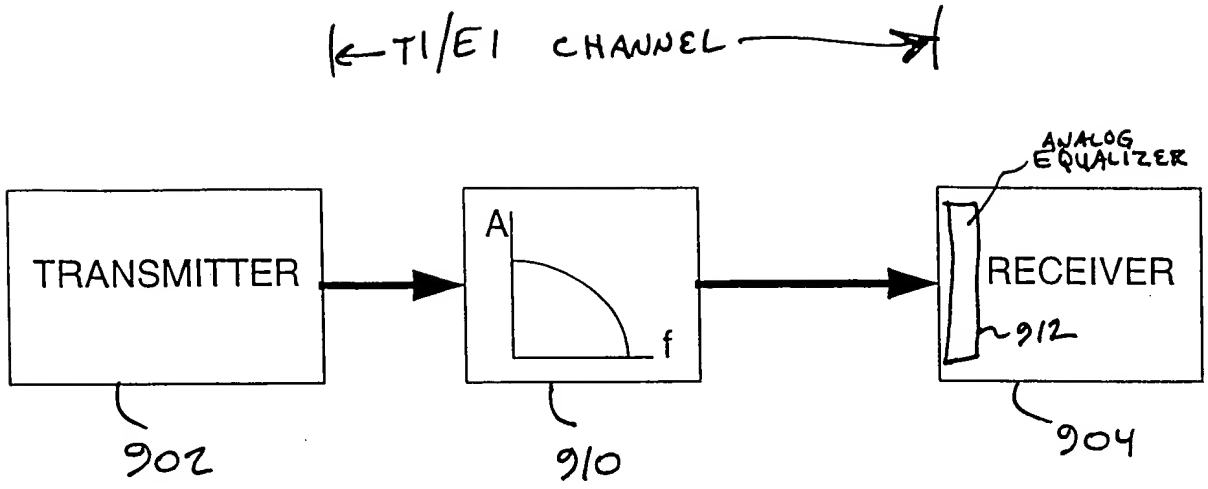


FIG. 8



PRIOR ART

FIG. 9